UNIVERSITY OF SOUTH FLORIDA

Defense of a Master's Thesis

Voltage droop analysis and mitigation in a STTRAM Last Level Cache

For the MSCS degree in Computer Science and Engineering

[illegible] Random Acc[illegible] technologies especially prefer[illegible] for a Last Level [illegible] farthest bank of [illegible] voltage droop across the STT RAM [illegible] and the [illegible] new cache [illegible] and make the write operati[illegible] single bank [illegible] in multiple physically separated loc[illegible]

THE PUBLIC IS INVITED

Examining Committee

Dr. Swaroop Ghosh, Ph.D., Co-Major Professor

Robert Bish[illegible]

[illegible]